REMARKS

Summary of Claim Status

Claims 1-15 are now pending in the present application with claims 1, 10, and 13 being independent. Applicants thank the Examiner for indicating that claims 13-15 are allowed and that claim 8 recites allowable subject matter. Claim 10 has been amended for clarity to more particularly point out that the recited recessed central region is defined by perimeter walls and a lower substrate floor. Applicants submit that this subject matter was included in the claims prior to the Final Office action and therefore does not necessitate an additional search. Moreover, the amendments made in Applicants' last response were made to address the Examiners' previous concerns regarding the clarity of the claims and did not affect the scope or subject matter recited in the claims. Accordingly, Applicants respectfully submit that the rejection by the Examiner based on entirely new references makes the finality of the present Office Action premature. Therefore, Applicants respectfully request withdrawal of the finality of the present Office Action or in the alternative entry and consideration of the amendment under 37 CFR 1.116(c).

Section 102 Rejections

The Examiner rejected claim 10 on a newly presented theory under 35 U.S.C. § 102(b) as being inherently anticipated by U.S. Patent No. 5,608,261 to Bhattacharyya. While Applicants do not dispute that by-pass capacitors are known to persons of ordinary skill in the art, Applicants do not acquiesce in the reasoning of the Examiner's rejection. The fact that the existence of by-pass capacitors is known cannot justify the rejection of claim 10.

Specifically, Bhattacharyya fails to teach or suggest each of the recited elements set forth in claim 10. The stepped gap formed in the substrate 10 shown in Bhattacharyya does not teach or suggest a recessed central region defined by perimeter walls and a lower substrate floor. In contrast with claim 10, Bhattacharyya employs metal plate 21 to form a floor for the package. Such a construction is entirely unsuitable for use in connection with the flip-chip package of the present invention. Therefore, Bhattacharyya fails to teach or suggest each of the elements recited in claim 10.

Claim 10 also stands newly rejected as anticipated by U.S. Patent No. 5,387,888 to Eda et al. ("Eda"). Applicants respectfully traverse this new ground of rejection because Eda fails to teach or suggest the combination recited in claim 10. Specifically, Eda discloses a substrate configuration that is suitable for operating a single transistor (i.e. transistor 9, 109, 209, 309) as a high-frequency amplifier. *See e.g.* col. 4, lines 41-59. By contrast, claim 10 recites *inter alia* "a plurality of contacts for providing electrical contact to an integrated circuit device. . ." Eda neither teaches nor suggests any such combination, at least for the reason that it fails to teach or suggest contacts for providing electrical contact to an integrated circuit." Therefore, Eda fails to teach or suggest each of the elements recited in claim 10. Further, none of the references of record render claim 10 obvious. Accordingly, Applicants submit that claim 10 is in condition for allowance.

Claims 1 and 5 have been rejected as anticipated by the newly presented U.S. Patent No. 5,892,280 to Crane et al ("Crane"). However, Crane fails to teach or suggest each of the elements of the combinations recited in claims 1 and 5,

and, on that basis, Applicants respectfully traverse the rejection of these claims. Claim 1 recites, *inter alia*, "an integrated circuit flipped … and placed against the recessed central region of the substrate… ." By contrast, Crane discloses semiconductor die 11 being mounted in a semiconductor die carrier 12. Nothing in Crane teaches or suggests an integrated circuit with contacts on its upper surface being flipped and placed against the recessed central region of a substrate. Therefore, for at least this reason, Crane fails to anticipate or render obvious claim 1.

Claim 5 depends from claim 1 and recites additional limitations. Therefore, claim 5 is novel and non-obvious over Crane for at least the reasons set forth in connection with claim 1.

Claims 1-3 and 9 are further rejected as being anticipated by newly identified reference U.S. Patent No. 6,272,020 to Tosaki et al. ("Tosaki"). However, Applicants respectfully submit that Tosaki is wholly inapplicable to claims 1-3 and 9. Specifically, claim 1 and its dependent claims 2-3 and 9 are directed to a flipped integrated circuit placed against a recessed central region. Tosaki, by contrast, discloses a flat substrate surface onto which a semiconductor device 2 is mounted on the flat upper surface of the substrate. Into a space 5 in the substrate is placed a group of capacitors 4. However, nothing in Tosaki teaches or suggests a flipped integrated circuit placed against a recessed central region as called for in claim 1.

Apparently perceiving that the capacitors 4 are truly not an "integrated circuit," the Examiner states that capacitors are "circuit devices" and that they are "integrated" with chips and substrates in Tosaki. However, Applicants respectfully submit that the term "integrated

circuit" has an established meaning in the art, which plainly excludes the capacitors 4 disclosed in Tosaki. Therefore, Tosaki fails to anticipate claim 1, and its corresponding dependent claims 2-3 and 9.

Section 103 Rejections

Claims 6 and 7 were rejected as being unpatentable over the combination of Crane and U.S. Patent No. 5,273,369. Applicants do not acquiesce in the Examiner's assertion that thermal conductive epoxy is the same as thermal grease or that the cap 21 of Crane meets the recited "heat spreader" limitation. Nevertheless, as set forth above, because Crane fails to teach or suggest each of the elements of the combination recited in their respective base claim, claim 1, and because Crane fails to remedy the deficiencies present in Crane, Applicants submit claims 6 and 7 are patentable over the asserted combination of references.

Claim 4 was rejected as being unpatentable over the combination of Tosaki and U.S. Patent No. 6,436,332. Without acquiescing in the Examiner's characterization of the '332 patent or any associated motivation to combine, Applicants respectfully submit that claim 4 is patentable over the applied combination of references at least for the reason that Tosaki fails to anticipate claim 1, as set forth above, and the '332 patent does not teach or suggest the elements lacking in Tosaki.

Claims 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhattacharyya in combination with U.S. Patent 6,368,514 to Metzler. The Examiner correctly observes that Bhattacharyya fails to teach or suggest the claimed structure of the recited capacitors. Applicants do not acquiesce in the Examiner's assertion that the batch thin

film capacitors described in Metzler teach the additional elements recited in claims 11 and 12. Nor do Applicants agree with the purported motivation to combine the Bhattacharyya and Metzler patents. Nevertheless, Applicants submit that these questions are moot in view of the fact that Bhattacharyya fails to teach or suggest each of the limitations recited in claim 10 as set forth above, and because claims 11 and 12 depend from claim 10 and recite further limitations, claims 11 and 12 are patentable over the applied combination of references for at least the same reasons set forth in connection with their base claim, claim 10. Therefore, Applicants respectfully request allowance of claims 4, 6-7, and 11-12.

CONCLUSION

In light of the above amendment and remarks, Applicants believe that claims 1-15 are in condition for allowance, and allowance of the application is therefore requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' agent at 408-879-4969.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Box AF, Commissioner for Patents, Washington, D.C. 20231, on March 12, 2003.

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